Demonstration of a vertical pin Ge-on-Si photo-detector on a wet-etched Si recess

Qing Fang, [1, 2*] Lianxi Jia, [1] Junfeng Song, [1, 3] Andy E. J. Lim, [1] Xiaoguang Tu, [1] Xianshu Luo, [1] Mingbin Yu, [1] and Guoqiang Lo[1]

[1]*Institute of Microelectronics, A*STAR (Agency of Science and Technology Research), 117685 Singapore*
[2]*Optoelectronic System Laboratory, Institute of Semiconductors, CAS, Beijing, 100083 China*
[3]*State Key Laboratory on Integrated opto-electronics, College of Electronic Science and Engineering, Jilin University, Changchun, 130023 China*
**fangq@ime.a-star.edu.sg*

Abstract: In this paper, we demonstrate a vertical pin Ge-on-Si photo-detector on a wet-etched Si recess on a SOI wafer. A 120nm-deep Si recess is etched on the SOI wafer with a 340nm-thick top Si layer by the TMAH solution. The measured results show that the responsivity is more than 0.60 A/W for TE polarization and is more than 0.65 A/W for TM polarization at 1550 nm wavelength. Compared to the photo-detector without the Si recess, the responsivities for both TE and TM polarizations are improved by ~10%. A low dark current of 170 nA is achieved at a bias voltage of −1 V. And, the 3dB-bandwidth at a bias voltage of −3 V is 21.5 GHz. This approach can be used to improve the coupling and absorption for high responsivity of photo-detector while maintain its high speed on a thick SOI platform based on the simulation results.

OCIS codes: (130.3120) Integrated optics devices; (130.0250) Optoelectronics; (250.0040) Detectors.

References and links

1. R. Kirchain and L. Kimerling, "A roadmap for nanophotonics," Nat. Photonics **1**(6), 303–305 (2007).
2. T. Tsuchizawa, K. Yamada, H. Fukuda, T. Watanabe, J. Kakahashi, M. Takahashi, T. Shoji, E. Tamechika, S. Itabashi, and H. Morita, "Microphotonics devices based on silicon microfabrication technology," IEEE J. Sel. Top. Quantum Electron. **11**(1), 232–240 (2005).
3. W. Bogaerts, P. Dumon, D. V. Thourhout, D. Taillaert, P. Jaenen, J. Wouters, S. Beckx, V. Wiaux, and G. R. Baets, "Compact wavelength-selective functions in Silicon-on-Insulator photonic wires," IEEE J. Sel. Top. Quantum Electron. **12**(6), 1394–1401 (2006).
4. P. Dong, W. Qian, H. Liang, R. Shafiiha, D. Feng, G. Li, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "Thermally tunable silicon racetrack resonators with ultralow tuning power," Opt. Express **18**(19), 20298–20304 (2010).
5. Q. Fang, J. F. Song, T. Liow, H. Cai, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Ultralow power silicon photonics thermo-optic switch with suspended phase arms," IEEE Photon. Technol. Lett. **23**(8), 525–527 (2011).
6. A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. Paniccia, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," Nature **427**(6975), 615–618 (2004).
7. T. Y. Liow, K. W. Ang, Q. Fang, J. F. Song, Y. Z. Xiong, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Silicon modulators and germanium photodetectors on SOI: monolithic integration, compatibility and performance optimization," IEEE J. Sel. Top. Quantum Electron. **16**(1), 307–315 (2010).
8. S. Klinger, M. Berroth, M. Kaschel, M. Oehme, and E. Kasper, "Ge-on-Si p-i-n photodiodes with a 3-dB bandwidth of 49 GHz," IEEE Photon. Technol. Lett. **21**(13), 525–527 (2009).
9. C. T. DeRose, D. C. Trotter, W. A. Zortman, A. L. Starbuck, M. Fisher, M. R. Watts, and P. S. Davids, "Ultra compact 45 GHz CMOS compatible germanium waveguide photodiode with low dark current," Opt. Express **19**(25), 24897–24904 (2011).
10. S. Liao, N. N. Feng, D. Feng, P. Dong, R. Shafiiha, C. C. Kung, H. Liang, W. Qian, Y. Liu, J. Fong, J. E. Cunningham, Y. Luo, and M. Asghari, "36 GHz submicron silicon waveguide germanium photodetector," Opt. Express **19**(11), 10967–10972 (2011).
11. B. Analui, D. Guckenberger, D. Kucharski, and A. Narasimha, "A fully integrated 20-Gb/s optoelectronic transceiver implemented in a standard 0.13-μm CMOS SOI technology," J. Solid-State Circuits **41**, 2945–2955 (2006).

#190854 - $15.00 USD Received 20 May 2013; revised 2 Jul 2013; accepted 2 Jul 2013; published 25 Sep 2013

12. Q. Fang, T. Y. Liow, J. F. Song, K. W. Ang, M. B. Yu, G. Q. Lo, and D. L. Kwong, "WDM multi-channel silicon photonic receiver with 320 Gbps data transmission capability," Opt. Express **18**(5), 5106–5113 (2010).
13. H. Pan, S. Assefa, W. M. J. Green, D. M. Kuchta, C. L. Schow, A. V. Rylyakov, B. G. Lee, C. W. Baks, S. M. Shank, and Y. A. Vlasov, "High-speed receiver based on waveguide germanium photodetector wire-bonded to 90nm SOI CMOS amplifier," Opt. Express **20**(16), 18145–18155 (2012).
14. D. Feng, W. Qian, H. Liang, B. J. Luff, and M. Asghari, "High-speed receiver technology on the SOI platform," IEEE J. Sel. Top. Quantum Electron. **19**(2), 3800108 (2013).
15. P. Dong, X. Liu, C. Sethumadhavan, L. L. Buhl, R. Aroca, Y. Baeyens, and Y.-K. Chen, " 224-Gb/s PDM-16-QAM modulator and receiver based on silicon photonic integrated circuits," presented at the Nat. Fiber Opt. Eng. Conf., OSA Tech. Dig., Anaheim, CA, 2013, Paper PDP5C.6.
16. T.-Y. Liow, J. F. Song, X. G. Tu, A. E.-J. Lim, Q. Fang, N. Duan, M. B. Yu, and G.-Q. Lo, "Silicon optical interconnect device technologies for 40 Gb/s and beyond," IEEE J. Sel. Top. Quantum Electron. **19**(2), 8200312 (2013).
17. D. Feng, W. Qian, H. Liang, C.-C. Kung, J. Fong, B. J. Luff, and M. Asghari, "Fabrication insensitive echelle grating in silicon-on-insulator platform," IEEE Photon. Technol. Lett. **23**, 284–286 (2011).
18. Q. Fang, J. F. Song, G. Zhang, M. B. Yu, Y. L. Liu, G. Q. Lo, and D. L. Kwong, "Monolithic integration of a multiplexer/demultiplexer with a thermo-optic VOA array on an SOI platform," IEEE Photon. Technol. Lett. **21**(5), 319–321 (2009).
19. D. Feng, S. Liao, P. Dong, N. N. Feng, H. Liang, D. Zheng, C.-C. Kung, J. Fong, R. Shafiiha, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide," Appl. Phys. Lett. **95**(26), 261105 (2009).

1. Introduction

Silicon photonic has been developed rapidly in the past decade, due to the perfect material properties and the mature fabrication process which is compatible with complementary metal-oxide-semiconductor (CMOS) technology. Many silicon photonics optical devices have been reported, such as passive devices, thermo-optic devices, electro-optical modulators/photo-detectors and integrated silicon photonic circuits [1–16]. Most of the above devices are fabricated on a submicron-thick SOI platform. However, these optical devices usually have an issue of polarization dependent loss, which is one of the main bottlenecks to retard the mass production and wide application of Si-based optical devices in the market.

In order to resolve the polarization issue, it is a reasonable choice to use a SOI platform with a thicker top Si layer, such as a micron-thick top layer. Some Si-based devices have been reported with good performances including a low polarization dependent loss on a SOI wafer with a micron-thick top Si layer [17,18]. The responsivity of vertical pin Ge-on-Si photo-detector (PD) is dependent on the Si thickness integrated under the Ge pattern. Once the Si thickness increases, most light will pass through the Si waveguide under the Ge pattern and hardly be coupled into the above Ge to be absorbed. Hence, the responsivity of this kind of PDs usually decreases if the Si waveguide height increases. Increasing the Ge length is one solution to improve its responsivity. However, it will decrease the PD speed because of the increase of the capacitance. Another solution is to reduce the thickness of the Si waveguide under the Ge to increase the coupling and absorption for higher responsivity. Kutora demonstrated a good horizontal pin Ge-on-Si PD with both high speed and high responsivity by reducing the Si thickness to 0.6 um on a 3um-thick Si waveguide using dry-etching process [19]. However, it is a challenge to epitaxially grow Ge on the dry-etched Si surface for most Ge Epi machines because the quality of Si surface formed by dry etching becomes poor. Moreover, it may be also a challenge to form a perfect Si/Ge transition waveguide because of the difference of etching rates of Si and Ge. The surface of Si formed by wet etching is fresh and it is easy to epitaxially grow the high-quality Ge. For a vertical pin Ge-on-Si PD, it is easier to precisely control the distance between P and N implantations and it can reduces the effect of the misalignment of lithography.

In this paper, we demonstrate a vertical pin Ge-on-Si PD on a Si recess formed by wet etching process for improving the responsivity while maintaining the performance of high speed. This PD is fabricated on a 340nm-thick SOI wafer and a 120nm-deep recess is formed by the Tetramethylammonium hydroxide (TMAH) solution. The measured results show that the responsivity is more than 0.6 A/W for TE polarization and is more than 0.65 A/W for TM

#190854 - $15.00 USD Received 20 May 2013; revised 2 Jul 2013; accepted 2 Jul 2013; published 25 Sep 2013

polarization at 1550 nm wavelength. Compared to the PD without the Si recess, the responsivities for both TE and TM polarizations are improved by ~10%. The 3dB-bandwidth at a bias voltage of –3 V is 21.5 GHz. According to the simulation results, the improvement of responsivity is more effective for the PD on thicker top silicon SOI platforms.

2. Device's design and fabrication

The lateral schematic diagram of a vertical pin Ge-on-Si PD on a Si recess is shown in Fig. 1. This device is designed on a SOI wafer with a 340nm-thick top Si layer. The Si crystal orientation is (100). The height of Silicon waveguide (H) is 340 nm and h is the height of Si recess. The bottom of Si recess is implanted with Boron as P-type implantation and the top of Ge is implanted with Phosphorous as N-type implantation. The thickness of Ge is 500 nm. L is the length of Ge. In our experiment, L has four kinds of splits, including 10 μm, 15 μm, 20 μm, 25 μm. A nano-taper Si waveguide is used as a mode converter at the beginning of 500nm-wide Si waveguide. Both butt and evanescent couplings are used for the light to couple into the Ge waveguide in this structure. Different responsivities can be realized by adjusting the value of h.

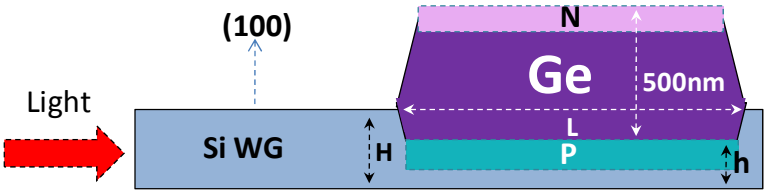

Fig. 1. Schematic structure of vertical Ge-on-Si PD on a Si recess

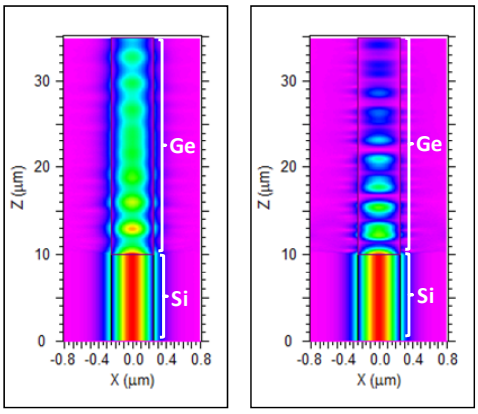

Fig. 2. Simulated optical field distribution in the vertical pin Ge-on-Si PD at 1550 nm (Left: h = 340 nm; Right: h = 102 nm).

The RSOFT commercial software can be used to estimate the relation between Ge absorption and the Si recess height. Based on the structure in Fig. 1, we assume that the refractive index of Ge is 4.280 and the absorption index of Ge is 0.013 at the wavelength of 1550 nm. At the same time, we assume the Ge waveguide width of 500nm to simplify the model. Two typical simulation results of optical field distribution are shown in Fig. 2. The Ge length is 25 μm and the height of Si waveguide is 340 nm. The heights of Si recess in left and right pictures are 340 nm and 102 nm, respectively. Figure 2 shows that the optical power obviously decreases with the reduction of the height of silicon recess. Hence, the height of Si recess can be designed to improve the responsivity of PD. Figure 3 shows the unabsorbed optical power vs. the height of Si recess at different lengths of PD. Besides the results on 340nm-high Si waveguides, we also achieve the simulation results on 500nm-high Si

#190854 - $15.00 USD Received 20 May 2013; revised 2 Jul 2013; accepted 2 Jul 2013; published 25 Sep 2013

waveguides. Reducing the height of Si recess is an effective solution to improve the responsivity of Ge-on-Si PD, especially for a thicker Si waveguide.

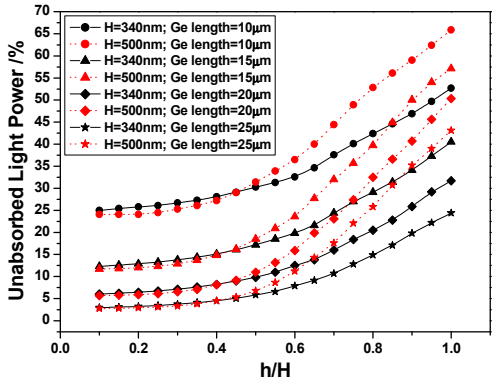

Fig. 3. Simulated unabsorbed optical power vs. h/H of Ge-on-Si PD

This vertical pin Ge-on-Si PD was fabricated on eight inch SOI wafers with a 340nm-thick silicon epitaxial layer and a 2um-thick buried oxide layer. The crystal orientation of the epitaxial silicon layer is (100). First, the channel Si waveguide was formed using a thin SiO_2 hard mask by dry etching process. The Si waveguide width in the Ge section was gradually tapered up to 15 μm and the Si taper is 100 μm long to reduce the optical loss. The SEM image of 200nm-wide Si tip is shown in Fig. 4(a). After the hard mask was stripped, another 100nm-thick SiO_2 layer was deposited as a screen layer for Si recess formation. The Si was etched in the TMAH solution to form the recess at the temperature of 70 °C, after the screen layer was opened in the recess area. Figure 4(b) is the image of Si recess formed by wet etching. The width and length of this recess are 5 μm and 10 μm, respectively. The inset shows the smooth wet-etched Si sidewall, which angle is ~54 ° derived from the crystal orientation of Si. The Si wet-etching process in TMAH is anisotropic. The Si wafers with different crystal orientations have different angles of the sidewall caused by TMAH etching. The propagation loss should not be seriously affected by the sidewall angle. However, compared to the dry-etched sidewall of ~90 degree, the return loss in our experiment should be quite low.

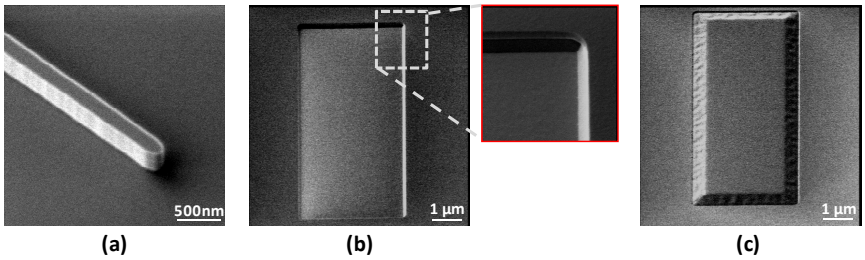

Fig. 4. (a) SEM image of Si nano-taper. (b) SEM image of Si recess formed by wet etching (inset: smooth sloped side wall formed by wet etching). (c) Ge pattern on the recess after Ge Epi process.

To form the Ge photodetectors, separate masks were used to implant boron into the photo-detector regions to form the *p* anode regions and the *p* + Ohmic contacts. The implants were activated via rapid thermal anneal of 1050 °C for 5 seconds prior to the selective epitaxial growth of Ge in an ultrahigh vacuum chemical vapor deposition (UHVCVD) epitaxy reactor. After growing a 50nm-thick SiGe buffer layer at 350 °C, Ge was selectively grown to a thickness of 500 nm at 550 °C. The *n* + ohmic contact was formed by implanting phosphorus into Ge, followed by an annealing at 500 °C for 5 min. For both of *p* + and *n* + Ohmic

#190854 - $15.00 USD Received 20 May 2013; revised 2 Jul 2013; accepted 2 Jul 2013; published 25 Sep 2013

contacts, double implantations with different energies and doses were used to reduce the contact resistance. Then, a TaN/Al metal stack was deposited and etched to form top and bottom contacts after contact holes opening. Finally, more than 100 μm Si cavity was etched to hold optical lensed fiber for coupling with the nano-taper of Si waveguide, instead of a polishing process. TEM images of Ge-on-Si PD on the Si recess are shown in Fig. 5. The inset of Fig. 5(a) shows the 220nm-high Si recess under the Ge film. A 50nm-high SiGe buffer layer is between the Si and the Ge. We also fabricated a Ge-on-Si PD without the Si recess, shown in Fig. 5(b).

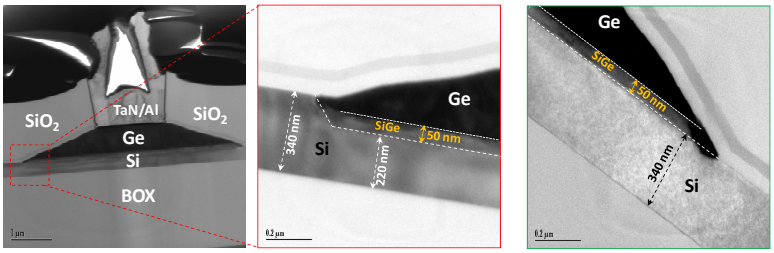

Fig. 5. (a) TEM image of Ge-on-Si PD on a Si recess. (b) TEM image of Ge-on-Si PD without a Si recess.

3. Characterization and analysis

After dicing, the end face of the chip doesn't need to polish because of the over 100μm-deep trench. An optical lensed fiber with 2.5 μm spot size is used to align with the nano-taper converter through the deep trench. The fiber-to-waveguide coupling loss and waveguide propagation loss were calibrated out of the responsivity measurements.

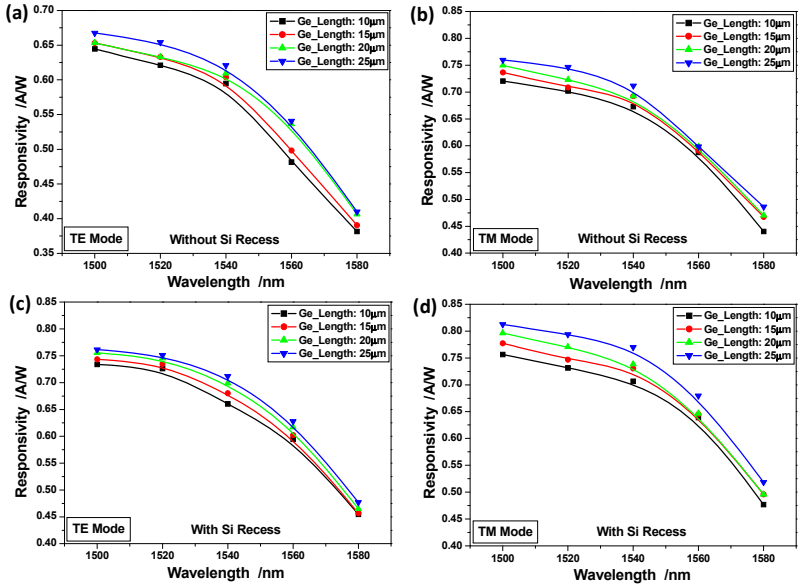

Fig. 6. (a) Measured responsivity of 5μm-wide Ge-on-Si PD on channel Si waveguide (without Si recess) with various lengths for TE mode. (b) Measured responsivity of 5μm-wide Ge-on-Si PD on channel Si waveguide (without Si recess) with various lengths for TM mode. (c) Measured responsivity of 5μm-wide Ge-on-Si PD on Si recess with various lengths for TE mode. (b) Measured responsivity of 5μm-wide G e-on-Si PD on Si recess with various lengths for TM mode.

#190854 - $15.00 USD Received 20 May 2013; revised 2 Jul 2013; accepted 2 Jul 2013; published 25 Sep 2013

As simulated before, there is an increase in the responsivity of Ge-on-Si PD on Si recess. The measured responsivities are shown in Fig. 6. Figure 6(a) and 6(c) are the results of responsivity without/with Si recess for TE mode, respectively. The responsivities of both PDs are dependent on the lengths of Ge and the wavelengths. At 1550nm, the responsivities of PDs on Si recess for TE mode is more than 0.60 A/W. Compared to the PD without Si recess, the responsivity of Ge-on-Si PD on Si recess increases ~10% for TE mode. The same tendency is shown in Fig. 6(b) and 6(d) for TM mode. The responsivities of PDs on Si recess for TM mode are more than 0.65 A/W at 1550 nm.

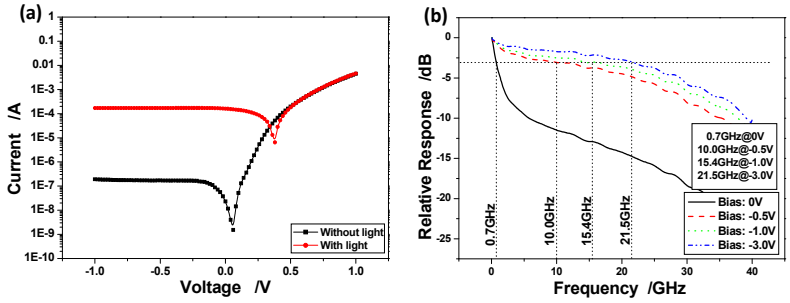

Fig. 7. (a) Dark current vs. voltage and illuminated current vs. voltage of a 5 μm × 10 μm Ge-on-Si PD on a Si recess. (b) Bandwidth of a 5 μm × 10 μm Ge-on-Si PD on a Si recess at various biases.

The dark current I-V characteristic of a 5 μm × 10 μm Ge-on-Si PD on a Si recess is shown in Fig. 7(a). A low dark current of 170 nA at a bias of −1 V is achieved. The corresponding current density is 3.4 nA/μm^2. When a −1.8dBm light of TE mode from the input lensed fiber is coupled to waveguide at 1550 nm, the corresponding illuminated current is shown in Fig. 7(a). The frequency response of this PD was measured by Agilent lightwave component analyzers (LCA). The RF signal generator is swept from 100 MHz to 40 GHz and the wavelength of applied optical signal is 1550 nm. The measured results at various biases are given in Fig. 7(b). The device demonstrates a 3-dB bandwidth of 21.5 GHz at a bias of −3 V. At other biases of 0V, −0.5 V and −1 V, the 3-dB bandwidths are 0.7 GHz, 10.0 GHz and 15.4 GHz, respectively. Further studies show that the speed of this device is limited by the RC constant. To further reduce the Ge width and the Ohmic contact resistance is an efficient solution to improve the speed.

4. Conclusion

We have demonstrated a vertical pin Ge-on-Si PD on a wet-etched Si recess to improve the responsivity. A 500nm-thick Ge layer epitaxially grows on a 120nm-deep Si recess on a SOI wafer with a 340nm-thick Si top layer. The responsivities of a 5 μm × 10 μm Ge-on-Si PD on a Si recess at 1550 nm are more than 0.6 A/W and 0.65 A/W for TE and TM modes, respectively, and its dark current is only 170 nA at a bias of −1 V. Compared to the PD without a Si recess, the increase of responsivity is ~10%. According to the simulation results, the improvement of responsivity is more efficient on a deeper silicon recess of a thicker SOI wafer and. Moreover, the kind of PD also maintains a high speed, 21.5 GHz at a bias of −3 V. The speed can be improved by reducing the Ge width and the Ohmic contact resistance.

Acknowledgments

The author would like to thank National Natural Science Foundation of China (Grant No. 61177064) and Singapore A*STAR SERC Grant No.1122804038 for support.

#190854 - $15.00 USD Received 20 May 2013; revised 2 Jul 2013; accepted 2 Jul 2013; published 25 Sep 2013