Wafer-Scale Dies-Transfer Bonding Technology for Hybrid III/V-on-Silicon Photonic Integrated Circuit Application

Xianshu Luo, Yuanbing Cheng, Junfeng Song, Tsung-Yang Liow, Qi Jie Wang, *Senior Member, IEEE*, and Mingbin Yu

(Invited Paper)

***Abstract*—In this paper, we review a variety of hybrid III/V-on-silicon integration platforms with focus on the optical coupling between III/V and silicon waveguides. Numerical simulations with regard to the coupling efficiency are conducted for various mode-overlapped and adiabatic-coupled structures for future design guideline. As a highlight, we show a novel wafer-scale dies-transfer bonding technology that features the merits of high bonding efficiency and process scalability for potential manufacturability of hybrid III/V-on-silicon photonic integrated circuit. Exemplary demonstration of up to 100 dies bonding to an 8-in processed silicon wafer is shown with ∼80% bonding yield, according to the C-mode scanning acoustic microscope characterization. As a proof-of-concept, hybrid silicon mode-locked lasers using the bonded wafer are demonstrated.**

***Index Terms*—Hybrid integrated circuits, silicon on insulator technology, wafer bonding, semiconductor lasers.**

I. Introduction

DUE to the insatiable data thirst in the information era, such as the applications of data center, cloud computing, social networking, etc., the electrical interconnection uses copper wires as the carrier for electrical signal transmission and distribution becomes bandwidth limited and also cause excessive electrical power consumption. On the other hand, optical interconnection [1]–[4] based on silicon photonics [5]–[10], where the signals are routed in low-loss optical waveguides, is proposed to address such distance-bandwidth-cost and power-consumption challenges owing to the advantages such as large bandwidth, immunity to electromagnetic interference, and low power consumption, etc. Most importantly, optical interconnects is expected to provide much larger data capacity using wavelength-division multiplexing technology. Furthermore, owing to the CMOS fabrication compatibility, large-scale photonic integrated circuits (PICs) on single silicon chip with compact footprint is potentially available with ultra-low power consumption, as well as significantly reduced cost.

Envisioned by Soref and Lorenzo in 1980s [11], silicon photonics have been developing very quickly along with a variety of prototype demonstrations including various silicon photonic building blocks such as optical passive filters [12], [13], optical switches [14], [15], high-speed silicon modulators [16], and large-bandwidth Ge-on-Si photodetectors [17]. Especially in recent years, first generation products are commercially available in market. Such demonstrated silicon photonic devices and technologies make ultimate optical interconnection a viable solution. Furthermore, the CMOS-compatible fabrication processes make it possible to integrate both electronics and photonics in a same chip, such as the most recent demonstration of optical microprocessor [18].

Regardless such explosion of silicon photonics, on-chip silicon laser has been a missing piece for a long time. Over the past decades, researchers worldwide have devoted great efforts for the development of silicon lasers, such as light emission through silicon material engineering [19], strained Ge lasers [20], silicon Raman laser [21], [22], heterogeneous integration of III/V gain materials through packaging method [23], III/V expitaxy growth on silicon wafer [24], [25], etc. However, the solution becomes more clear only when the demonstrations of various hybrid silicon lasers [26]–[43] through III/V-to-silicon wafer bonding technology [44]–[50]. Although the performances of the demonstrated hybrid lasers are not as perfect as their III/V counterpart, the advantages of hybrid silicon laser is also very obvious, such as the potential of monolithic integration with silicon PICs.

Although the history of III/V lasers on silicon wafer through wafer bonding technology was very long with various demonstrations [51]–[54], the first hybrid silicon laser was demonstrated in 2005 [26]. The significance of the hybrid silicon integration is the light output from silicon waveguide, which indicates the integration feasibility of III/V material with silicon PICs. Another merit of such hybrid silicon integration is the less constrained alignment requirements to the wafer bonding technology as the optoelectronic devices are fabricated after wafer bonding, and the alignment to silicon wafer is achieved via lithographic process. Following this pioneering work, various hybrid silicon lasers with different designs and enhanced device performances are demonstrated, such as Fabry-Perot

Manuscript received February 01, 2016; revised April 05, 2016; accepted April 05, 2016. This work was supported by A∗STAR SERC Future Data Center Technologies Thematic Strategic Research Program under Grant 112 280 4038, and A∗STAR Science and Technology Joint Funding Program under Grant 122 331 0076.

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Digital Object Identifier 10.1109/JSTQE.2016.2553453

TABLE I
THE MAJOR BONDING TECHNOLOGY FOR HYBRID SILICON PHOTONICS INTEGRATION

	Process description	Pros	Cons
W2W molecular bonding	• O2 plasma assisted bonding directly on silicon waveguides	• Strong bond strength • Less thermal concern from the interlayer oxide	• Small bonding tolerance • III/V and silicon wafer mismatch • Waste of high cost InP wafer
D2W molecular bonding	• O2 plasma assisted bonding with oxide interlayer using pick-and-place flip-chip bonding	• Hydrophilic molecular bonding with strong bonding strength • Cost saving by minimize the III/V waste	• Small bonding tolerance • Contamination and surface deactivation limiting the bonding yield
	• O2 plasma assisted bonding with oxide interlayer using batch processing	• Wafer-level process for manufacturability • Scalability with silicon wafers	• Small bonding tolerance
D2W adhesive bonding	• Adhesive bonding using BCB	• Large bonding tolerance • Wafer-level process for manufacturability	• Requirement of controllable thickness and flatness of the polymer layer • Poor thermal dissipation due to the low thermal conductivity of the BCB material
	• Adhesive bonding using metal	• Large bonding tolerance • Enhanced thermal resistant	• Reduced process compatibility due to potential metal contamination • Potential optical loss due to metal absorption

lasers [27], microring lasers [34], [55], distributed Bragg reflector lasers [36], [56], distributed feedback lasers [31], [56]–[58], mode-locked lasers (MLLs) [32], [57], [59], etc. Other than hybrid silicon lasers, various high-performance hybrid III/V-on-silicon devices/circuits using wafer bonding method are also demonstrated [60]–[65], showing the robustness of such important enablement technology.

With regard to the bonding technology for hybrid silicon photonic integration, there are mainly two different types, namely the molecular bonding using van der Waals forces [48], [49], and the adhesive bonding with assistance of an adhesion layer, such as polymer [47], [50], [66], [67] or metal [68], [69]. Considering the thermal budget after silicon PICs, the bonding temperature is limited to be less than 400 °C. In general, the molecular bonding is able to achieve very high bonding strength owing to the strong van der Waals forces. The trade-off is the stringent requirements to the bonding surface, such as flat, smooth, and extremely clean surface in order to avoid any surface contamination [70]. Besides, the bonding interface also tends to trap the generated gas by-product of H_2 and H_2O and form the interfacial voids, thus significantly degrade the bonding quality and yield. Alternatively, strong hydrophilic molecular bonding can be used with improved bonding quality by covering both silicon and InP wafers with oxide layer. Such oxide layer also helps to absorb the generated gas by-product to minimize the void generation. In contrast, the adhesive bonding with the assistance of the adhesion layer can largely release the bonding constraints with increased bonding yield. However, there are also different issues for such adhesive bonding, such as the less efficient heat dissipation by using polymer or the process contamination by using metal.

On the other hand, in order to facilitate the potential manufacturability of hybrid silicon integrated circuits, various wafer-scale III/V-to-Si bonding method are proposed and demonstrated, such as the full 6 inch InP-to-silicon bonding method [71], the flip-chip bonding using pick-and-place method [48], die-to-wafer collective bonding [72], etc. However, while wafer-to-wafer bonding tends to cause III/V wafer waste as only very small portion of the silicon wafer requiring III/V devices, the number of the bonding dies using flip-chip bonding through pick-and-place method tends to be limited due to the bonding surface contamination and de-activation. Thus, wafer-scale die-to-wafer bonding technology with robust process scalability is highly demanded. In Table I, we summarize and compare currently available major bonding methods which all aim for potential manufacturability.

The rest of the paper is organized as follows. We first review different hybrid silicon photonics integration platforms, focusing on the light coupling schemes from III/V waveguide to silicon waveguide. Numerical simulations with different designs are provided for future design guideline. We then review the developed wafer-scale dies-transfer bonding technology with the demonstration of more than 100 III/V dies bonding to an 8 inch processed silicon wafers. Characterization of the bonding quality through CSAM and cross section investigation are performed, suggesting a bonding yield of $\sim$80% with strong bonding interface. Demonstrations of hybrid MLL using such wafer-scale dies-transfer bonding technology are shown as an example. Finally, we summarize this paper.

II. HYBRID III/V-ON-SILICON INTEGRATION PLATFORMS

There are various designs of hybrid integration platforms with regard to the waveguide coupling structure between III/V and silicon waveguides. Despite the design complication, we here classify them into two different types depending on the optical mode confinement within III/V and silicon waveguides [43], namely overlapped hybrid mode structure, and adiabatic-coupled structure. In the overlapped hybrid mode structure, the III/V waveguide layer and silicon waveguide layer are vertically aligned with only a thin oxide interlayer sandwiched between them, thus forming a hybrid mode which propagates inside the overlapped waveguides. Whereas for the adiabatic-coupled structure, the III/V and silicon waveguides are separated with each other along the waveguide direction. In such case, the III/V layer only serves as the gain medium and most of the optical mode can sufficiently overlap with the gain region. The light coupling from III/V waveguide to silicon waveguide is through waveguide mode transformer, such as waveguide inverse tapers.

TABLE II
STACKED LAYERS OF THE III/V WAVEGUIDE STRUCTURES

Material	Layer thickness (nm)	Refractive index
Cladding oxide	300	1.45
InP	1500	3.1681
InAlGaAs SCH	160	3.4564
InGaAsP MQW	134	3.53
InP	110	3.1681
2 × InGaAsP	2 × 7.5	3.2818
2 × InP	2 × 7.5	3.1681
InP	10	3.1681
Interlayer oxide	50	1.45
	Silicon device layers	

TABLE III
THE KEY SIMULATION PARAMETERS

Parameter	Values (μm)
Si waveguide width, wSi	0.5
Si waveguide taper width, wSi1T1	2
Si inverse taper width, wSi1T2	0.2
Si waveguide taper width, wSi2	1.5
Si inverse taper width, wSi2T2	0.2
InP waveguide width, wInP	4
InP inverse taper width, wTInP	0.3

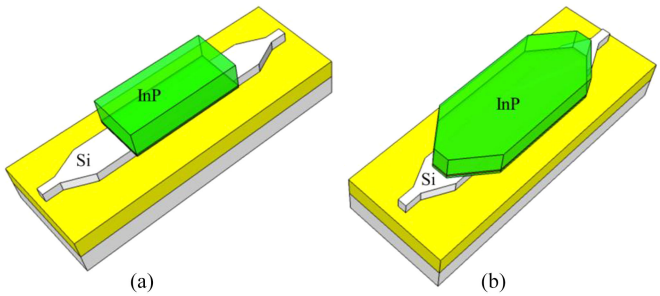

Fig. 1. The schematics of two basic overlapped hybrid mode structures. (a) Conventional structure (A1), and (b) tapered structure (A2).

In the section, we will investigate these hybrid integration platforms by numerical simulation with regard to the optimization of coupling efficiency between III/V and silicon waveguides. In order for fair comparison, the InP multiple quantum well (MQW) waveguide structures are with the identical stacked layers as shown in Table II, including the layer thickness and the refractive index. Other representative simulation parameters are listed in Table III, while all the tapered waveguide are optimized with sufficient lengths in order for minimized transition loss.

Fig. 1(a) shows the most common design (type A1) of the overlapped hybrid mode structure. In such design, the light confinements in III/V waveguide and silicon waveguide solely depend on the waveguide thickness. Taking InP MQW structure as an example, the optical effective index is typically $\sim$ 3.2. In order to achieve this effective refractive index for silicon waveguides for sufficient light coupling, the corresponding silicon waveguide thickness needs to be sufficiently high [27]. Fig. 2 shows the simulated coupling efficiency as function of silicon waveguide thickness. With the mainstream silicon waveguide thickness of 220 nm, the efficiency is less than 10% due to the large mismatch of the effective refractive index. As the silicon waveguide thickness increases, the coupling efficiency increases and it reaches ~80% with waveguide thickness of 600 nm. However, the optical confinement in InP MQW decreases as the increased silicon waveguide thickness, subsequently affecting the mode overlapping with the gain region. Thus, for such overlapped hybrid mode structure, it is required to consider the trade-off between the coupling efficiency and the optical mode overlapping for efficient light amplification.

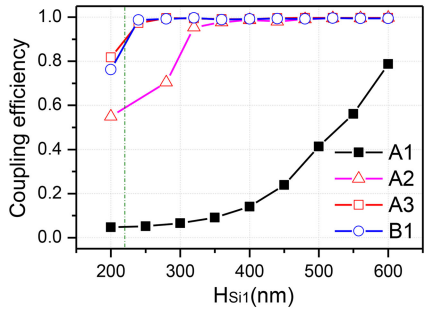

Fig. 2. The simulated coupling efficiency from III/V waveguide to silicon waveguide with regard to the silicon waveguide thickness for different types of coupling schemes. The coupling efficiency is significantly increased by using waveguide tapers.

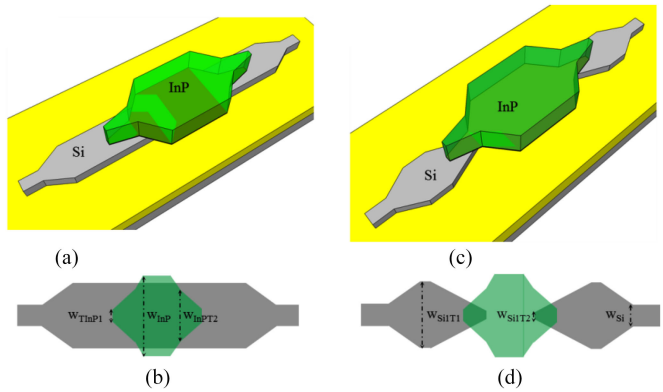

Fig. 3. The perspective and top-view schematics of the dual-layered waveguide structures. (a), (b) The mode-overlapped structure (A3), and (c), (d) the adiabatic-coupled structure (B1).

Alternatively, it is possible to design III/V waveguide mode transformer for efficient light coupling without the necessity to increase the silicon waveguide thickness [73]. The simplest waveguide mode transformer is the waveguide taper by adiabatically changing the waveguide width (type A2), as shown in Fig. 1(b). The light confined in III/V waveguide is gradually pushed to silicon waveguide when the III/V waveguide width gradually reduces. The simulated light coupling efficiency is also plotted in Fig. 2. Even with silicon waveguide thickness of only ~220 nm, the light coupling efficiency is able to reach ~60%. The coupling efficiency increases significantly with the increase of the silicon waveguide thickness. It achieves $>$ 90% and becomes stable after the silicon waveguide thickness is $>$ 300 nm.

Practically, in order to enhance the coupling efficiency, various waveguide mode transformers with different designs are demonstrated. Fig. 3(a), (b) shows the perspective and top views

of the design with two stages of linear adiabatic tapers (type A3) [37]. In our simulation, the width of the first stage taper is adiabatically changed from 4 μm to 2 μm, while the second taper is changed from 2 μm to 0.3 μm. The waveguide taper lengths, as mentioned, are all optimized with minimum transition loss. Fig. 2 shows the simulated coupling efficiency with comparing to those of other designs. The optical coupling efficiency increases to ~90% with silicon waveguide thickness of 220 nm. Thus, by using such coupling structure, it is feasible to integrate hybrid III/V devices directly on the mainstream silicon photonic wafers, thus being able to adopting the existing silicon photonics device library.

For a hybrid silicon laser, another design consideration is the overlapping of the optical mode with MQW gain region, which affects the modal gain and thus the lasing performances. For the mode-overlapped structure, there is a design trade-off for the silicon waveguide thickness between the light coupling and the sufficient optical overlapping with the MQW layer. With thick silicon waveguide design, it generally requires longer laser cavity in order to for sufficient modal gain, and resulting in high power consumption. Thus, in order to largely confine the optical mode in InP waveguide, and increase the overlapping with MQW layer, while without degradation the coupling efficiency, the adiabatic-coupled structure (B1) is proposed and demonstrated [74], as show in Fig. 3(c) and (d). In such design, the III/V waveguide and the silicon waveguide do not overlap along the waveguide direction, except the adiabatic coupling region. The optical mode in the hybrid section is mainly guided in the III–V waveguide, and experiences a high optical gain in the central region of the laser structure. While the optical coupling efficiency is only dependence on the adiabatic coupling design. Yet, we observe there is no significant difference of the optical light coupling efficiency comparing to that of overlapped structure (A3) as shown in Fig. 2. This suggests that the optical coupling is dominantly affected by the adiabatic taper design as both structures have the same design of the waveguide tapers in our simulation.

Another critical parameter that affects coupling efficiency is the III/V waveguide taper width. Unlike the silicon waveguide which is fabricated in CMOS line with advanced photolithography such as 248 nm or 193 nm lithography with an achievable waveguide tip as narrow as 100 nm in width, the post III/V optoelectronic fabrication is relatively difficult to utilizing such advanced photolithography due to process compatibility, thus with a relatively wider waveguide taper. The optical coupling efficiency from the III/V waveguide to silicon waveguide thus significantly affected. Fig. 4 shows the simulated optical coupling efficiency as the function of III/V taper width for the adiabatic-coupling structure B1. The optical coupling efficiency gradually decreases from 0.99 to 0.98 with the III/V taper with increase from 100 nm to 600 nm. Then it decreases very fast from 0.98 to 0.85 with the taper width increasing to 1 μm. Such decreased coupling efficiency could significantly affect the laser performance, such as resulting in high threshold current and low output power. As an example, Fig. 4(b), (c) shows the simulated mode field transition coupling from InP waveguide to silicon waveguide, respectively with $wTInP = 0.3\,\mu\mathrm{m}$, and $wTInP = 1\,\mu\mathrm{m}$. With small waveguide tip, the optical field is gradually coupled from the InP layer to the silicon layer, with

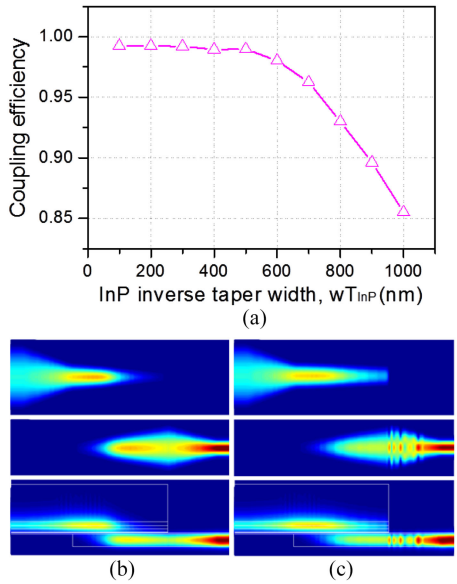

Fig. 4. (a) The simulated coupling efficiency in the silicon waveguide as function of the InP inverse taper width. The mode filed transition from InP waveguide to silicon waveguide with (b) $wTInP = 0.3\,\mu\mathrm{m}$, and (c) $wTInP = 1\,\mu\mathrm{m}$.

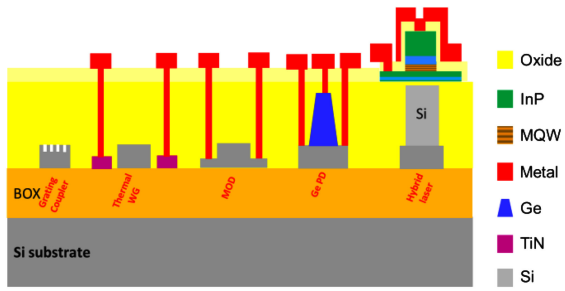

Fig. 5. Conceptual schematic of the hybrid III/V-on-Si PIC, including silicon modulator, Ge photodetector, thermo-tunable waveguide, and hybrid silicon laser.

minimum transition loss. In contrast, with the increased waveguide tip width, the optical intensity is difficult coupling from InP waveguide, and radiates from the InP tip, with increased coupling loss.

For most of the demonstrated hybrid devices, the III/V waveguide is closely located atop of silicon waveguide, usually with only a thin oxide bonding layer between them. Such platform is unable to integrate other silicon photonic devices, such as Ge photodetector which is normally sitting on silicon waveguide with 500 nm thickness. Thus, novel III/V-to-Si coupling scheme that facilitates hybrid silicon PICs is demanded, such as multi-layered waveguide coupling structures [37], [75]. Fig. 5 shows a conceptual schematic of a hybrid III/V-on-Si PIC, including standard silicon photonic passive and active devices, as well as hybrid III/V-on-Si laser. In such a platform, the silicon waveguide thickness is 220 nm and the Ge photodetector is 500 nm in thickness sitting on the silicon waveguide, which targets to use the existing silicon photonic library devices. In such integration platform, the distance between III/V layer and the waveguide device layer is normally larger than 500 nm. Thus in order to efficiently coupling the light from III/V to

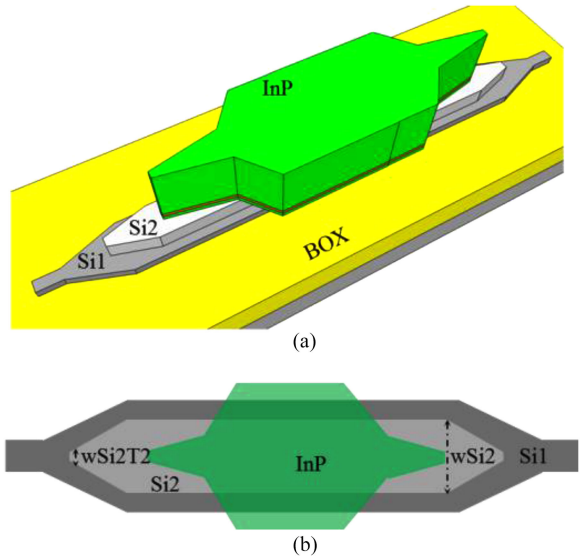

Fig. 6. The (a) perspective and (b) top-view of a triple-layered waveguide structure (A4) proposed for hybrid silicon PIC.

silicon waveguide, a multi-layered waveguide structure is required [37], [75], [76].

Fig. 6(a) and (b) shows respectively perspective and top views of the triple-layered waveguide structure for hybrid silicon PICs. In additional to the silicon waveguide layer with 220 nm thickness and the III/V layer as the gain medium, there is another silicon transition layer sandwiched between them which is formed by silicon epitaxial growth. From the technical point of view, such silicon epitaxial growth process is mature enough and is able to selectively grow thick silicon layer. However, in the case of hybrid integration, such transition silicon layer needs to be optimized take into account both integration feasibility and the coupling efficiency. Besides, we show here only as an example of the overlapped hybrid-mode structure, while it is also feasible to have similar design with adiabatic-coupled structure.

Fig. 7 shows the simulated coupling efficiency from III/V waveguide to silicon waveguide with regard to the thickness of the transition silicon layer. The key simulation parameters for the transition silicon waveguide design are also listed in Table III. With thin transition silicon layer of below 400 nm, the optical coupling efficiency is as high as 95%. As the silicon thickness is higher than 400 nm, the optical coupling efficiency starts to decrease gradually till ~80% with thickness of 800 nm, and decrease significantly when the transition thickness further increases. With the transition silicon thickness larger than 1.1 μm, the light coupling from III/V waveguide to silicon waveguide is only ~10%. Fig. 7(b) and (c) shows the optical field profiles in the transmission plane respectively for silicon transition layer thickness of 200 nm and 1.5 μm. When the transition silicon thickness is small, the optical field confines in InP waveguide, and gradually coupled to the transition silicon waveguide, and finally to silicon waveguide. However, when the thickness of the transition silicon waveguide increases, the optical mode dominates inside the transition silicon layer. It is difficult to efficiently push the light into the underneath silicon waveguide with high radiation loss in the thick waveguide tip region, and significantly reducing the coupling efficiency. Thus, for advanced

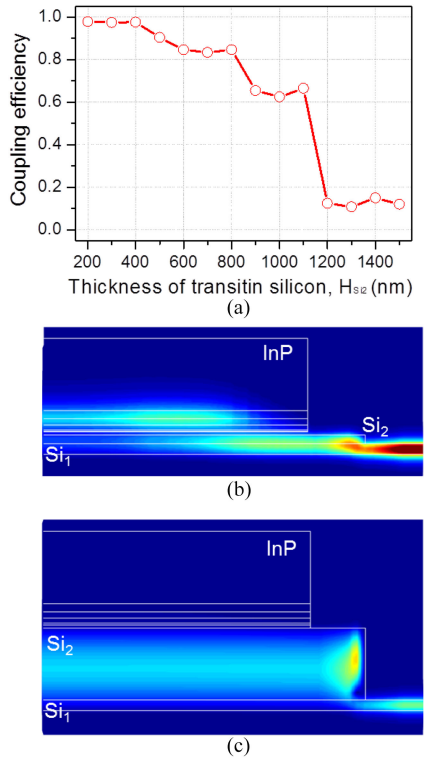

Fig. 7. (a) The simulated coupling efficiency from III/V to silicon waveguide as function of transition silicon waveguide thickness. Simulated mode field profile with transition silicon thicknesses of (b) 200 nm and (c) 1.5 μm.

integration scheme which requires the transition silicon thickness greater than 800 nm, even complicated coupling structure might be required.

III. Wafer-Scale Dies-Transfer Bonding Technology

In order to facilitate the manufacturability of hybrid III/V-on-silicon photonic integration, we proposed and demonstrated a wafer-scale dies-transfer bonding technology [43]. Fig. 8 shows the key process steps of such bonding technology. In general, it comprises the following three major stages, namely:

1) Silicon wafer preparation, including silicon integration wafer fabrication, and bonding surface treatment;
2) InP dies preparation, including III/V wafer dicing, dies distribution to silicon handle wafer, batch processing such as sacrificial layer removal, bonding surface treatment, etc.; and
3) Wafer-scale dies-transfer, including wafers physical contact through notch alignment, dies-to-wafer pre-bonding, dies transferring from handle wafer to silicon wafer, and post-bonding annealing.

The silicon integration wafers are fabricated with commercially available 200 mm SOI wafers in IME's CMOS lines, following the standard silicon photonic integration process [77], [78]. There are various silicon photonics platform, including passive integration [79], active integration [80], multi-layered waveguide integration [81], etc. However, for all kinds of silicon photonic integration platforms, the silicon devices are all cladded with oxide layer. Thus, in order to ensure surface flatness and smoothness for molecular bonding, surface

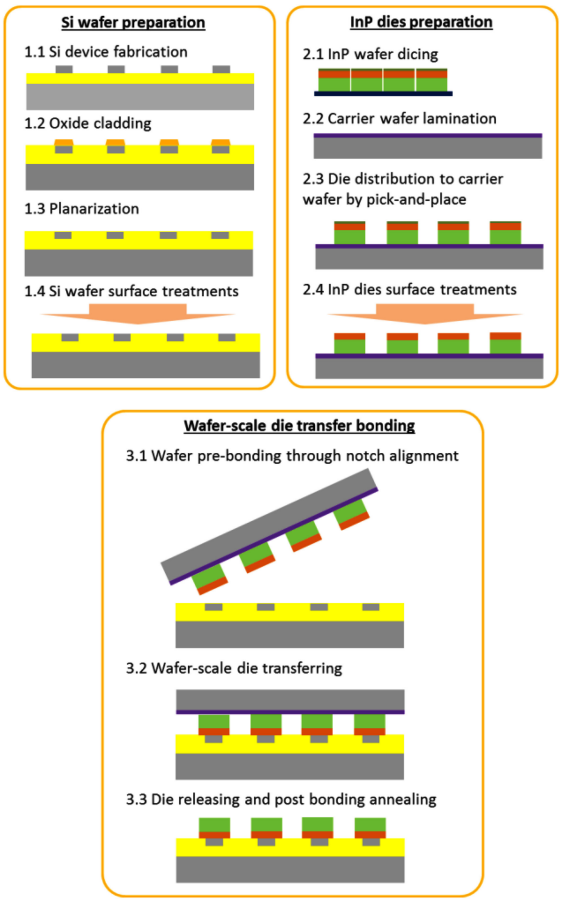

Fig. 8 Process flow of the wafer-scale dies-transfer bonding technology.

planarization including multiple oxide etch-back processes and chemical mechanical polishing (CMP) is applied [42], [43]. The surface roughness after the CMP can be with RMS of ∼0.4 nm, which is more suitable for wafer molecular bonding [70].

The InP dies preparation starts from the wafer dicing into small dies with pre-determined die size using commercially available wafer dicing machines. The InP MQW wafers are specifically designed for hybrid silicon laser operating in 1550 nm wavelength range and grown by a commercially available III/V epitaxial wafer supplier. In order to minimize the wafer chipping, we need to carefully choose the dicing blade with suitable thickness as well as optimize the dicing speed. Fig. 9(a) shows the photograph of a diced 2 inch InP MQW wafer on a dicing tape, while Fig. 2(b) shows the zoom-in microscope view of the dicing lane with the minimized chipping. In order to avoid the contamination to the bonding surface such as particle attachment during wafer dicing, the InP MQW wafer is protected by a sacrificial InGaAs cap layer, which will be removed by wet etching prior bonding.

In parallel, a proprietary adhesion material is laminated to a silicon handle wafer in order for InP dies temporary bonding. The choice of the adhesion material is very critical and will significantly affect the bonding yield. We need to consider following two trade-off criteria [43]: 1) The adhesion should be strong enough to avoid III/V dies peeling off from the handle wafer during the subsequent III/V dies batch processing, and 2) The adhesion should not be excessively strong to ensure the III/V dies to be successfully released and transferred to the silicon wafer.

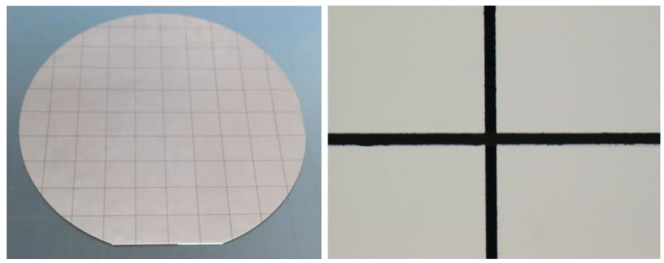

Fig. 9. (a) The diced 2 inch InP wafer on dicing tape with $5\,\mathrm{mm} \times 5\,\mathrm{mm}$ die size. (b) The optical microscope zoom-in view of the dicing lane, showing minimized chipping.

The III/V dies are then temporary bonded to the handle wafer through programmable distribution by pick-and-place method. Taking into account the wafer-level die distribution of the silicon device wafer, the III/V dies position coordinates can be predetermined. The pick-and-place process in our proposed method only serves to distribute the III/V dies to the handle wafer under optimized bonding force without flipping the chips. While in flip-chip bonding, the pick-and-place process directly bonds the dies to the silicon wafer [48]. Furthermore, the pick-and-place bonding heads is directly contacted with the III/V die top surface. Thus, the sacrificial InGaAs cap layer also helps to avoid the possible contamination from the bonding heads to the bonding surface. After that, all the dies attached to the handle wafer are able to be processed in a batch mode with various surface treatments, including InGaAs cap layer wet etching, wafer pre-clean, wafer N2 drying, and O2 plasma activation.

Prior the physical contact of the wafers for molecular bonding, both silicon wafer and III/V attached handle wafer are performed with standard wet cleaning in order to ensure the cleanness of the bonding surface. For silicon integration wafer, we perform standard SPM clean for 10 minutes followed with SC1 clean with mega sonic for 5 minutes. For III/V dies attached handle wafer, we first perform the sacrificial InGaAs cap layer etch in H_3PO_4 solution for 1 minute, followed with surface clean in NH_4OH solution for 2 minutes. After that, both wafers are performed with O_2 plasma activation in a RIE chamber for 1 minute, followed with DI wafer rinsing and N_2 drying.

The III/V dies and silicon wafer are then physically contacted for pre-bonding through wafer notch alignment between silicon wafer and the handle wafer. In order to minimize the misalignment of the notch alignment, we design an 8 inch wafer clamping ring in order to fix both wafers without shifting. A notch alignment pin is also design to assist the localization of both wafers. Fig. 10(a) and (b) shows the EVG bonder plate attached with the designed wafer clamping ring, respectively without and with bonding wafers. Practically, the D2W bonding alignment accuracy is mainly affected by the notch alignment, which is performed manually with a relatively large misalignment of $\pm 500\ \mu$m, comparing to the misalignment of only $\pm 5\ \mu$m from the programmable reconfiguration by pick-and-place process [43]. The alignment accuracy can experimentally be traced by

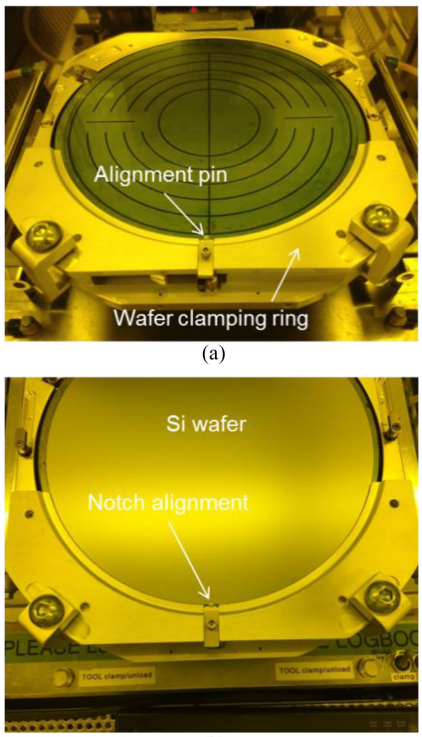

Fig. 10. The designed wafer clamping ring with alignment pin for notch alignment (a) without and (b) with bonding wafers.

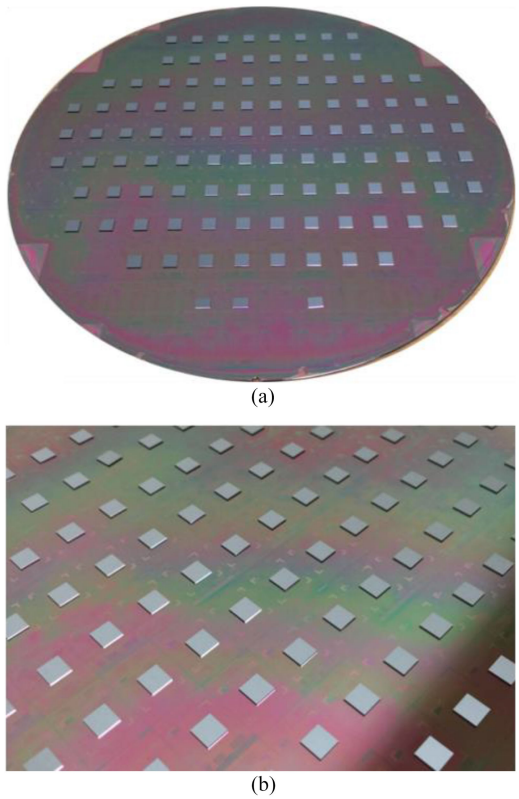

Fig. 11. (a) Photo image of a processed 8 inch silicon wafer with over 100 InP dies bonded on it. (b) Perspective zoom-in image of the bonded dies. The InP die size is $5\,\mathrm{mm} \times 5\,\mathrm{mm}$, with each of them located in the silicon die defined by four "L" shapes.

designed "L" shapes located in the four corners of the silicon dies. In the future design, the alignment accuracy can be further increased by designing alignment marks in both handle wafer and silicon wafer. We expect that by using such alignment method during wafer-to-wafer bonding, the alignment accuracy can be improved to few tens of micrometers. However, such misalignment can be easily compensated during post optoelectronic fabrication by using relatively large-sized III/V dies, as the alignment of the III/V devices to the silicon waveguide device is determined through photolithography.

The physically contacted wafers are then placed in a 200 mm EVG bonder to perform pre-bonding for 2 minutes with 7000 N mechanical force and 0.005 mbar vacuum levels in the chamber. After pre-bonding, the III/V dies are then released from the handle wafer and transferred to the silicon device wafer. Finally, the III/V dies bonded silicon wafer is placed back to the EVG bonder for post bonding annealing at 300 °C for 12 hours, with applying 1000 N mechanical force.

Fig. 11(a) shows the photo image of a processed 8 inch silicon wafer with over 100 InP dies bonded on it, whereas Fig. 11(b) shows the zoom-in view of the wafer center region. There are in total 104 dies survived out of 112 dies after pre-bonding. Although there is oxide non-uniformity suggested by different colors in the wafers, we don't expect it would significantly affect the bonding quality as the D2W bonding mostly depending on the local surface condition. In contrast, W2W bonding would be largely affected by such global film non-uniformity, which will generate bonding void. This is a successful demonstration of bonding over 100 InP MQW dies to a processed silicon device wafer, which benefits from the bonding process optimization comparing to our previous work which shown 104 bulk InP dies bonding to silicon test wafer [43].

Fig. 12(a)–(c) shows the C-mode scanning-acoustic microscope (CSAM) of the bonded wafer, and the zoom-in views of two specific dies (in red circles). After CSAM, some of the dies which are not firmly bonded peel off, leaving all the dies with relatively high bonding strength. In CSAM, the bright color suggests the defects, which is the area with poor bonding quality. In the bonded wafer, most of the dies show tiny defects along the die edge, which are attributed to the die chipping from the wafer dicing as observed in Fig. 9(b). Some of the dies with large bonding void (large bright area) are due to possible surface contamination, which results in the failure of the bonding. If we define the successful D2W bonding with $> 90\%$ bonded area for each individual die, the bonding yield is estimated to be $\sim$80% (90 out of 112 dies). The bonding yield can be further improved by minimizing the wafer surface contamination and increasing the bonding force. Actually we perform the wafer bonding in IME's MEMS line for back end of the line processing, which is expected with potential high contamination. Furthermore, the existing EVG 520 bonder is only with a maximum bonding force of 7 kN, which correspond to a pressure of only $\sim$2.5 N/mm^2. Thus, by using another advanced EVG Gemini bonder with maximum bonding force of 70 kN in IME's Class 10 CMOS line for front-end of line processing, we expect the bonding yield could be enhanced with up to 90%. Fig. 12(d), (e) shows the full-sized SEM and zoom-in TEM cross sectional

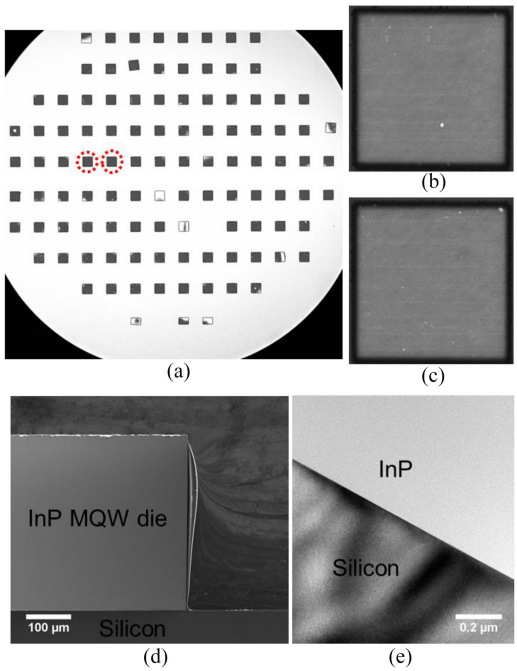

Fig. 12. (a) The CSAM image of the bonded wafer. (b), (c) Zoom-in CSAMs of two bonded dies without any major defects. The (d) full-sized SEM and (e) zoom-in TEM cross-sectional views of the bonded die.

views of a typical bonded die, which suggest a very high-quality bonding.

Comparing to other bonding technologies that also aims for potential massive III/V-on-Si integration [48], [67], the significance of such wafer-scale dies-transfer bonding technology is the batch processing of all the III/V bonding dies by temporary bonding them to the silicon handle wafer. This eliminates the separated processing to individual III/V dies, thus greatly enhancing the bonding efficiency with unlimited number of dies. Furthermore, such bonding method is scalable with any other sized silicon wafer using commercially available bonding tools, thus facilitating the advanced silicon photonic fabrication progress even with 300 mm wafers.

IV. Passively Mode-Locked Hybrid Silicon Laser

Semiconductor passively MLLs are capable of generating stable ultra-short optical pulses with low time jitter, high extinction ratios, and low chirp. It has opened up a broad range of applications from high speed optical communications to medical imaging. By combing the low-loss and low-dispersion characteristics of silicon waveguide and high gain III/V material, the performance of such hybrid silicon MLLs [82]–[85] can be significantly improved due to the reduction of spontaneous emission in the laser cavity. For instance, by using very long low-loss silicon waveguide cavity, it enables semiconductor MLLs to generate ultra-short optical pulses with low repetition rate and low time jitter, which is challenging for a III–V MLL owing to the short carrier lifetime in its long cavity. As we know, the radio-frequency (RF) linewidth is directly proportional to the reciprocal of the square of the laser cavity length, which means that the timing jitter for MLL with longer cavity can be greatly reduced. In this section, we show a demonstration of

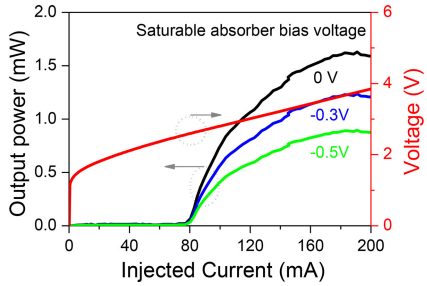

Fig. 13. Measured P–I and V–I curves of the fabricated hybrid silicon MLL with different biased voltages of the SA section under CW operation at 20 °C. The differential resistance was is nearly ∼9 Ω.

a passively MLL with low loss silicon waveguide leading to a low phase noise operation based on the developed hybrid silicon integration platform.

The III/V device fabrication starts with InP substrate removal, following the process that was described in [43]. Although there are various hybrid III/V-on-silicon integration platforms as illustrated in Section II, we are currently unable to fabricate III/V inverse tapers, due to the photolithography limitation of III/V optoelectronic fabrication. Thus, in current demonstration, we choose the overlapped hybrid mode structure A1 as shown in Fig. 1(a). The laser cavity is formed by the III–V/Si hybrid mode waveguide with the cavity length as same as that of III–V waveguide and silicon waveguide. Cleaved facets at both waveguide ends are made as the reflection mirror. The thickness of the silicon waveguide is 500 nm with an inter-layer oxide thickness of ∼50 nm after CMP. The MLL consists of a gain section with a length of 1150 μm, and a saturable absorber (SA) region with length of 60 μm, which are separated by a 20-μm-long electrical isolation region with higher than 1 kΩ isolation resistance. All of gain section, SA region, and the isolation region are made up of the same III/V material. The SA absorbs the light in the cavity upon applying a reverse or zero biased voltage to the SA region, while the gain section amplifying the light upon forward biased. Practically, the isolation region also serves as a SA with no biased voltage. In order to balance the optical modal gain and the light coupling to silicon waveguide in such a mode-overlapped structure, the confinement factor in the III/V region for our device is designed to be about 5% [43].

The device is characterized at 20 °C with the chip sitting on a temperature controlled copper submounts by a thermoelectric cooler. The temperature control accuracy is ±0.1 °C. The laser optical output is collected by an optical integrating sphere located in front of the cleaved facet. Fig. 13 shows the output optical power versus injection current (P–I) and voltage versus injection current(V–I) curves of the fabricated MLL with different biased voltages to the SA section under continuous-wave (CW) operation. The turn-on voltage is about 1.14 V and the series differential resistance is nearly ∼9 Ω. The typical threshold current with a zero biased 60-μm-long SA section is about 80 mA. A maximum single facet CW output power of about 1.6 mW is achieved when the injection current is 180 mA. When the injection current at the gain section is fixed, the output power reduces with the increase of the SA biased voltage due to the quantum confinement stark effect of the MQW. However,

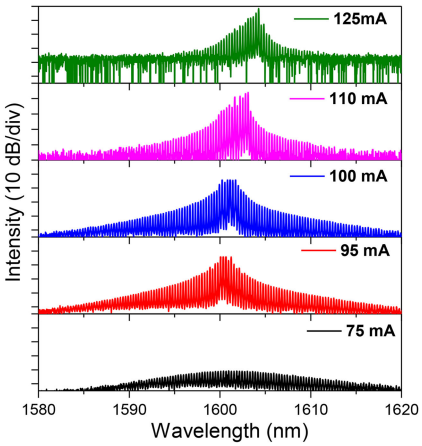

Fig. 14. Measured optical spectra of the hybrid silicon MLL at different injection currents to the gain section. The SA section is zero biased.

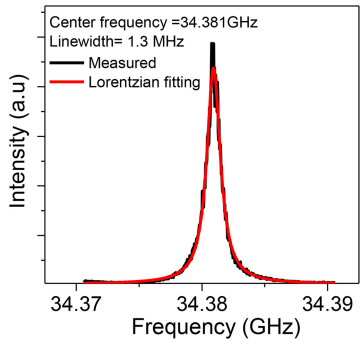

Fig. 15. Measured RF spectrum of the hybrid silicon MLL at 100 mA injection current and −0.5 V SA biased voltage. The RBW is 100 KHz in the measurement.

we don't observe obvious threshold current increase when the bias voltage of the SA section increases. This is because the additional average cavity loss induced by the change of the SA bias voltage is much smaller than the overall average cavity loss. Besides, there is electrical crosstalk between the gain and SA sections due to insufficiently large isolation resistance.

The output light from the laser diode is coupled to an optical spectrum analyzer (OSA) by a lensed single mode fiber for spectrum analysis. The measured optical spectra at different injection currents when the SA section is zero biased are shown in Fig. 14. When the injection current is 75 mA, which is below the threshold injection current of the device, the output is amplified spontaneous emission (ASE) spectra. By measuring the extinction ratio of the peaks and valleys of the ASE spectra around 1600 nm, the modal loss is estimated to be 16.3 cm^{-1} using the Hakki-Paoli method:

$$\langle \alpha \rangle = \frac{1}{L} \ln \left(\frac{1}{R} \frac{1+\sqrt{S}}{1-\sqrt{S}} \right) \tag{1}$$

where *L* is the cavity length, *S* is the ratio of intensity peak to valleys in the ASE resonances, and *R* is the mirror reflectivity.

The lasing wavelength is centered at 1600 nm at 95 mA and shifts to longer wavelengths at higher current levels due to device heating. The lasing peak wavelength shift rate is ∼ 0.14 nm/mA. A 3-dB optical bandwidth as large as 2.1 nm with the wavelength centered at ∼1601 nm is obtained at the injection current of 100 mA.

Based on these results, the temporal pulse width of the MLL is estimated to be 1.28 ps, assuming that the generated optical pulse is Fourier-transform-limited and the shape of the pulse is with a sech^2 function.

Passive mode locking of the device achieved when the gain section (I_{gain}) is forward biased and the SA section is reverse (V_{sa}) or zero biased. The mode locking behavior is characterized with a 40 GHz bandwidth photodiode followed by a 50 GHz bandwidth RF spectrum analyzer. The measured RF spectrum of the hybrid silicon MLL at $I_{\text{gain}} = 100\,\text{mA}$ and $V_{\text{sa}} = -0.5\,\text{V}$ is shown in Fig. 15. The repetition frequency is about 34.381 GHz and the signal-to-noise ratio (SNR) is larger than 20 dB, measured with the resolution bandwidth (RBW) of 100 kHz, giving clear evidence of passive mode locking. The measured 3-dB RF linewidth of the injection locked laser is about 1.3 MHz by Lorentzian fitting the RF spectrum. When I_{gain} is further increased to more than 200 mA, the mode-locking operation becomes unstable with 3-dB RF linewidth more than 200 MHz and the SNR is greatly reduced indicating that the laser is not properly locked.

As noted in Ref. [86], MLL with tunable repetition rate provides the flexibility for network application and allows for later upgrades to different transmission standards. The repetition rate of the MLL can be written in the following equation:

$$f = \frac{mc}{2\left(n_g L_g + n_a L_a\right)} \tag{2}$$

where n_g, n_a are respectively the group refractive indices in the gain section and SA section. L_g, L_a are respectively the length of the gain section and SA section. c is the speed of light in vacuum and $m = 1$ is the harmonic index.

As we know, the group refractive index of the waveguide can be reduced by applying a forward current to inject carriers (free-carrier plasma dispersion effect) or increased by a reverse bias to increase the electric field (electro-optic effect or stark effect). Thus, by changing I_{gain} or V_{sa}, the repetition rate of the MLL can be dynamically tuned, as shown in Fig. 16. The tuning slopes are 1.72 MHz/mA and −1.2 MHz/V, respectively.

To further characterize the noise performance of the device, we measure the single sideband (SSB) phase noise spectra around the carrier frequency of 34.381 GHz. The measurement results of the root-mean-square (RMS) timing jitter and the corresponding SSB phase noise spectra are shown in Fig. 17. For the free running hybrid silicon MLL with I_{gain} of 100 mA and V_{sa} of −0.5 V, the RMS timing jitter from offset frequency range of 100 Hz -100 MHz is 3.84 ps, which is nearly ten times smaller than that of our previous fabricated III–V MLL on silicon substrate [41]. Such improvement is attributed to the utilization of low loss silicon waveguide to form the laser cavity as well as better temperature control of the device during the measurement.

In order to reduce the phase noise and timing jitter thus fulfill the applications such as analog-to-digital converters (ADC) and high resolution spectroscopy, alternative method such as CW optical injection is adopted [41]. In such CW optical injection scheme, a master CW tunable laser with 100 kHz optical linewidth and output power of −2 dBm is used. The tunable

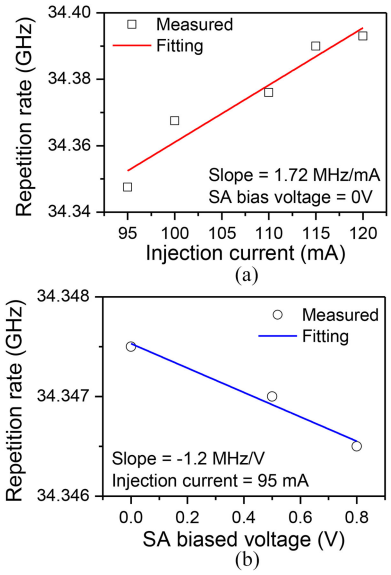

Fig. 16. Measured repetition rate as functions of (a) the gain injection current at SA biased voltage of −0.5 V, and (b) the SA biased voltage at gain injection current of 95 mA. The RBW during measurement is 100 KHz.

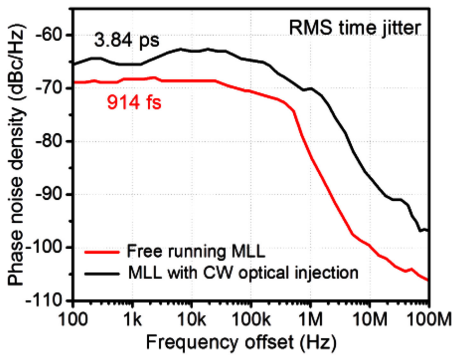

Fig. 17. The SSB phase noise traces for the free running silicon hybrid MLL, and silicon hybrid MLL with CW optical injection. $I_{\rm gain}$ is 100 mA and $V_{\rm sa}$ is −0.5 V during the traces measurement.

laser's wavelength is tuned to coincide with the center of the spectrum of MLL and lock the MLL by pulling its wavelength towards the master laser's wavelength. As shown in Fig. 17, the RMS timing jitter in the range of 100 Hz −100 MHz is reduced to 914 fs by using such method.

V. Conclusion

In summary, we reviewed various hybrid III/V-on-silicon integration platforms with main focus on the waveguide coupling structure between III/V and silicon waveguides. Numerical simulations of the coupling efficiency for these coupling structures are provided as future design guideline. Multiple-layered waveguide structure for advanced hybrid silicon photonic integration with active silicon photonic devices, such as silicon modulator, Ge photodetector, etc., are conceptually illustrated, with numerical simulation of the coupling efficiency using multiple layered waveguide structures. A proprietary wafer-scale die-transfer bonding technology is highlighted, showing the merits of high bonding efficiency with unlimited bonding dies and the scalability to any sized silicon wafers, which enables potential manufacturability of large-scale hybrid silicon photonic integration. As an example, we show a demonstration of up to 100 InP dies bonded to an 8 inch processed silicon photonic wafer, with a bonding yield of ∼80%. Using such bonded wafer, we demonstrate a hybrid silicon MLL with an output power of ∼1.6 mW, a repetition rate of ∼34.381 GHz, and a RF linewidth of ∼1.3 MHz. By using CW optical injection the RMS time jitter of the MLL is reduced from 3.84 ps to 914 fs, making it attractive for the applications such as photonic ADC and high resolution spectroscopy.

Acknowledgment

The authors would like to thank Dr. G.-Q. Lo, NanoPhotonics Program Director for the guidance and the research direction provided. They would also like to thank Dr. L. Ding from the Institute of Material Research and Engineering, Agency for Science, Technology and Research for the help of numerical simulation of various hybrid silicon integration platforms and valuable discussion.

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